We claim:

1. A system to enhance buffering low-voltage flash memory, comprising:

a multiple of thin gate-oxide transistors; and

an input buffer receptive to an enabling signal, an input signal, and an inhibiting signal, wherein the input buffer includes a component that inhibits semiconductor breakdown of the multiple of thin gate-oxide transistors when the inhibiting signal is at a low voltage level.

2. The system of claim 1, wherein the component includes a first connection, a second connection, and a third connection, wherein the first connection is coupled to the inhibiting signal, wherein the second connection is coupled to the input signal, wherein the third connection presents the input signal when the inhibiting signal is at a first predetermined level.

3. The system of claim 2, wherein the third connection of the component refrains from presenting the input signal when the inhibiting signal is at a second predetermined level so as to inhibit semiconductor breakdown of the multiple of thin gate-oxide transistors when the input signal is at an undesired high voltage level.

4. The system of claim 1, further comprising a voltage sensor receptive to the input signal and a pumped signal, wherein the voltage sensor produces a sensed signal at a third predetermined level when the input signal is at a desired high voltage level, otherwise the voltage sensor produces the sensed signal at a fourth predetermined level.

5. The system of claim 4, further comprising an inhibiting circuit receptive to the pumped signal and the sensed signal, wherein the inhibiting circuit produces the inhibiting signal.

6. An input buffer for a low-voltage flash memory device, comprising:

an input stage having a first connection, a second connection, and a third connection, wherein the first connection is receptive to an inhibiting signal, wherein the second connection is receptive to an input signal, wherein the input stage inhibits the input signal from being presented at the third connection when the inhibiting signal is at a predetermined level; and

an output stage having a first connection and a second connection, wherein the first connection is coupled to the third connection of the input stage, and wherein the second connection presents the input signal to the low-voltage flash memory device.

7. The input buffer of claim 6, further comprising a resistor coupled to the second connection of the input stage, wherein the resistor limits a current when the input signal comprises a signal generated from an electrostatic discharge.

8. The input buffer of claim 7, further comprising a first clamping circuit coupled to the resistor to clamp the input signal to a voltage supply, wherein the first clamping circuit enhances an electrostatic-discharge test that is applied to the low-voltage memory device.

9. The input buffer of claim 7, further comprising a second clamping circuit coupled to the resistor to clamp the input signal to ground, wherein the second clamping circuit enhances an electrostatic-discharge test that is applied to the low-voltage memory device.

10. The input buffer of claim 7, further comprising a third clamping circuit coupled to the third connection of the input stage to clamp the input signal being presented at the third connection of the input stage to a voltage supply, wherein the third clamping circuit enhances a charge-device-model test that is applied to the low-voltage memory device.

11. The input buffer of claim 7, further comprising a fourth clamping circuit coupled to the third connection of the input stage to clamp the input signal being presented at the third connection of the input stage to ground, wherein the fourth clamping circuit enhances a charge-device-model test that is applied to the low-voltage memory device.

12. An input buffer for a low-voltage flash memory device, comprising:

an input stage having a gate, a drain, and a source, wherein the gate is receptive to an inhibiting signal, wherein the drain is receptive to an input signal, wherein the input stage inhibits the input signal from being presented at the source when the inhibiting signal is at a predetermined level; and

an output stage having a first connection and a second connection, wherein the first connection is coupled to the source of the input stage, and wherein the second connection presents the input signal to the low-voltage flash memory device.

13. The input buffer of claim 12, further comprising a first p-channel transistor having a gate, a drain, a source, and a bias, wherein the gate is receptive to the inhibiting signal, wherein the source is coupled to the source of the input stage, and wherein the bias is coupled to the source of the first p-channel transistor.

14. The input buffer of claim 13, further comprising a second p-channel transistor having a gate, a drain, a source, and a bias, wherein the gate is receptive to

the inhibiting signal, wherein the source is coupled to the drain of the first p-channel transistor, wherein the bias is coupled to the drain of the second p-channel transistor.

15. The input buffer of claim 14, further comprising a resistor having a first connection and a second connection, wherein the first connection is coupled to the drain of the second p-channel transistor, wherein the second connection is coupled to a voltage supply.

16. The input buffer of claim 15, wherein the coupling between the source of the first p-channel transistor and the drain of the input stage defines a node, wherein the first p-channel transistor and the second p-channel transistor act to prevent the node from floating when the inhibiting signal is at the predetermined level.

17. An input buffer for a low-voltage flash memory device, comprising:

an input stage having a gate, a drain, and a source, wherein the gate is receptive to an inhibiting signal, wherein the drain is receptive to an input signal, wherein the input stage inhibits the input signal from being presented at the source when the inhibiting signal is at a predetermined level; and

an output stage having an inverter that includes a first connection and a second connection, wherein the first connection is coupled to the source of the input stage, and wherein the second connection presents the input signal to the low-voltage flash memory device.

18. The input buffer of claim 17, wherein the inverter includes an n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the input stage, wherein the source is coupled to ground, and wherein the drain presents an inverted input signal.

19. The input buffer of claim 18, wherein the inverter further includes a p-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the input stage, wherein the source is coupled to the drain of the n-channel transistor.

20. The input buffer of claim 19, further comprising an enabling transistor having a gate, a drain, and a source, wherein the gate is receptive to an enabling signal, wherein the drain is coupled to a voltage supply, wherein the source is coupled to the drain of the p-channel transistor.

21. The input buffer of claim 20, wherein the enabling transistor includes a p-channel transistor.

22. An input buffer for a low-voltage flash memory device, comprising:

an input stage having a transistor that includes a gate, a drain, and a source, wherein the gate is receptive to an inhibiting signal, wherein the drain is receptive to an input signal, wherein the transistor inhibits the input signal from being presented at the source when the inhibiting signal is at a first predetermined level;

an output stage having an inverter that includes a first connection and a second connection, wherein the first connection is coupled to the source of the transistor, and wherein the second connection presents the input signal to the low-voltage flash memory device; and

a voltage sensor to trigger when the input signal is at a second predetermined level, wherein the voltage sensor is receptive to a pumped signal and the input signal.

23. The input buffer of claim 22, wherein the voltage sensor includes a triggering stage receptive to the input signal, wherein the triggering stage includes a

first portion that has a set of p-channel transistors that includes:

a first p-channel transistor having a gate, a drain, a source, and a bias, wherein the gate is coupled to a first resistor, wherein the bias is coupled to the input signal, wherein the first resistor is coupled to a voltage supply;

a second p-channel transistor having a gate, a drain, a source, and a bias, wherein the gate is coupled to a second resistor, wherein the drain is coupled to the second resistor and the source of the first p-channel transistor, wherein the bias is coupled to the input signal;

a third p-channel transistor having a gate, a drain, a source, and a bias, wherein the gate is coupled to a third resistor, wherein the source is coupled to the input signal, wherein the drain is coupled to the third resistor and the source of the second p-channel transistor, and wherein the bias is coupled to the input signal; and

wherein the triggering stage includes a second portion that has a set of n-channel transistors that includes:

a first n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the pumped signal, wherein the source is coupled to ground;

a second n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the pumped signal, wherein the source is coupled to the drain of the first n-channel transistor;

a third n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the pumped signal, wherein the source is coupled to the drain of the second n-channel transistor;

a fourth n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the pumped signal, wherein the source is coupled to the drain of the third n-channel transistor;

a fifth n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the pumped signal, wherein the source is coupled to

the drain of the fourth n-channel transistor; and

a sixth n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the pumped signal, wherein the drain is coupled to the source of the first p-channel transistor, and wherein the source is coupled to the drain of the fifth n-channel transistor.

24. The input buffer of claim 23, further comprising a set of metal options that includes:

a first metal option having a first connection and a second connection, wherein the first connection is receptive to the input signal, and wherein the second connection is coupled to the source of the third p-channel transistor;

a second metal option having a first connection and a second connection, wherein the first connection is coupled to the source of the third p-channel transistor, and wherein the second connection is coupled to the drain of the third p-channel transistor;

a third metal option having a first connection and a second connection, wherein the first connection is coupled to the source of the second p-channel transistor, and wherein the second connection is coupled to the drain of the second p-channel transistor;

a fourth metal option having a first connection and a second connection, wherein the first connection is coupled to the drain of the fifth n-channel transistor, and wherein the second connection is coupled to the source of the fifth n-channel transistor;

a fifth metal option having a first connection and a second connection, wherein the first connection is coupled to the drain of the fourth n-channel transistor, and wherein the second connection is coupled to the source of the fourth n-channel transistor;

a sixth metal option having a first connection and a second connection,

wherein the first connection is coupled to the drain of the third n-channel transistor, and wherein the second connection is coupled to the source of the third n-channel transistor;

a seventh metal option having a first connection and a second connection, wherein the first connection is coupled to the drain of the second n-channel transistor, and wherein the second connection is coupled to the source of the second n-channel transistor; and

an eighth metal option having a first connection and a second connection, wherein the first connection is coupled to the drain of the first n-channel transistor, and wherein the second connection is coupled to the source of the first n-channel transistor.

25. The input buffer of claim 23, further comprising an inverting stage that includes:

a first inverting stage that includes:

a first inverter that includes:

a seventh n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the drain of the sixth n-channel transistor, wherein the source is coupled to ground;

a fourth p-channel transistor having a gate, a drain, a source, and a bias, wherein the gate is coupled to the gate of the seventh n-channel transistor, wherein the source is coupled to the voltage supply, wherein the drain is coupled to the drain of the seventh n-channel transistor, and wherein the bias is coupled to the voltage supply;

a second inverter that includes:

an eighth n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the drain of the seventh n-channel transistor, wherein the source is coupled to ground;

a fifth p-channel transistor having a gate, a drain, a source, and a bias, wherein the gate is coupled to the gate of the eighth n-channel transistor, wherein the source is coupled to the voltage supply, wherein the drain is coupled to the drain of the eighth n-channel transistor, and wherein the bias is coupled to the voltage supply;

a second inverting stage that includes:

a third inverter having a first connection and a second connection, wherein the first connection is coupled to the drain of the eighth n-channel transistor; and

a fourth inverter having a first connection and a second connection, wherein the first connection is coupled to the second connection of the third inverter.

26. The input buffer of claim 25, further comprising a delay stage to reject undesired noise that includes:

a first delay circuit that includes:

a first metal option having a first connection and a second connection, wherein the first connection is coupled to the drain of the eighth n-channel transistor;

a second metal option having a first connection and a second connection, wherein the first connection is coupled to the voltage supply, wherein the second connection is coupled to the second connection of the first metal option;

a sixth p-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the second connection of the first metal option, wherein the drain is coupled to the source, wherein the source is coupled to the voltage supply;

a second delay circuit that includes:

a third metal option having a first connection and a second

connection, wherein the first connection is coupled to the drain of the eighth n-channel transistor;

a fourth metal option having a first connection and a second connection, wherein the first connection is coupled to ground, wherein the second connection is coupled to the second connection of the third metal option;

a ninth n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the second connection of the third metal option, wherein the drain is coupled to the source, wherein the source is coupled to ground;

a third delay circuit that includes:

a fifth metal option having a first connection and a second connection, wherein the first connection is coupled to the drain of the eighth n-channel transistor;

a sixth metal option having a first connection and a second connection, wherein the first connection is coupled to the voltage supply, wherein the second connection is coupled to the second connection of the fifth metal option;

a seventh p-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the second connection of the fifth metal option, wherein the drain is coupled to the source, wherein the source is coupled to the voltage supply;

a fourth delay circuit that includes:

a seventh metal option having a first connection and a second connection, wherein the first connection is coupled to the drain of the eighth n-channel transistor;

an eighth metal option having a first connection and a second connection, wherein the first connection is coupled to ground, wherein the second connection is coupled to the second connection of the seventh metal option; and

a tenth n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the second connection of the seventh metal option,

wherein the drain is coupled to the source, wherein the source is coupled to ground.

27. An input buffer for a low-voltage flash memory device, comprising:

an input stage having a transistor that includes a gate, a drain, and a source, wherein the gate is receptive to an inhibiting signal, wherein the drain is receptive to an input signal, wherein the transistor inhibits the input signal from being presented at the source when the inhibiting signal is at a first predetermined level;

an output stage having an inverter that includes a first connection and a second connection, wherein the first connection is coupled to the source of the transistor, and wherein the second connection presents the input signal to the low-voltage flash memory device; and

an inhibiting circuit to selectively produce the inhibiting signal, wherein the inhibiting circuit is receptive to a pumped signal and a sensed signal.

28. The input buffer of claim 27, wherein the inhibiting circuit includes a first n-channel transistor having a gate, a drain, and a source, wherein the gate is receptive to the sensed signal, wherein the drain presents the inhibiting signal, wherein the source is coupled to ground.

29. The input buffer of claim 28, wherein the inhibiting circuit includes a second n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to an inverted sensed signal, wherein the source is coupled to ground.

30. The input buffer of claim 29, wherein the inhibiting circuit includes a first p-channel transistor having a gate, a drain, a source, and a bias, wherein the gate is coupled to the drain of the second n-channel transistor, wherein the source is receptive to the pumped signal, wherein the drain is coupled to the drain of the first n-channel transistor, and wherein the bias is receptive to the pumped signal.

31. The input buffer of claim 30, wherein the inhibiting circuit includes a second p-channel transistor having a gate, a drain, a source, and a bias, wherein the gate is coupled to the drain of the first n-channel transistor, wherein the source is receptive to the pumped signal, wherein the drain is coupled to the drain of the second n-channel transistor, and wherein the bias is receptive to the pumped signal.

32. An input buffer for a low-voltage flash memory device, comprising:

an input stage having a first n-channel transistor that includes a gate, a drain, and a source, wherein the gate is receptive to an inhibiting signal, wherein the drain is receptive to an input signal, wherein the input stage inhibits the input signal from being presented at the source when the inhibiting signal is at a low level;

an output stage to present the input signal to the low-voltage flash memory device, wherein the output stage includes:

a second n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the first n-channel transistor, wherein the source is coupled to ground, and wherein the drain presents an inverted input signal;

a first p-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the first n-channel transistor, and wherein the drain is coupled to the drain of the second n-channel transistor; and

a second p-channel transistor having a gate, a drain, and a source, wherein the gate is receptive to an enabling signal, wherein the source is coupled to a voltage supply, wherein the drain is coupled to the source of the first p-channel transistor.

33. An input buffer for a low-voltage flash memory device, comprising:

an input stage having a first n-channel transistor that includes a gate, a drain,

and a source, wherein the gate is receptive to an inhibiting signal, wherein the drain is receptive to an input signal, wherein the input stage inhibits the input signal from being presented at the source when the inhibiting signal is at a low level;

an output stage to present the input signal to the low-voltage flash memory device, wherein the output stage includes:

a second n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the first n-channel transistor, wherein the source is coupled to ground, and wherein the drain presents an inverted input signal;

a first p-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the first n-channel transistor, and wherein the drain is coupled to the drain of the second n-channel transistor; and

a second p-channel transistor having a gate, a drain, and a source, wherein the gate is receptive to an enabling signal, wherein the source is coupled to a voltage supply, wherein the drain is coupled to the source of the first p-channel transistor;

a voltage sensor to trigger when the input signal is at a first high level, wherein the voltage sensor is receptive to a pumped signal and the input signal to produce a sensed signal; and

an inhibiting circuit to selectively produce the inhibiting signal, wherein the inhibiting circuit is receptive to the pumped signal and the sensed signal.

34. A method for buffering a low-voltage flash memory device, comprising:

transferring by an input stage having a gate, a drain, and a source, wherein the gate is receptive to an inhibiting signal, wherein the drain is receptive to an input signal, wherein the input stage inhibits the input signal from being presented at the

source when the inhibiting signal is at a predetermined level; and

outputting by an output stage by inverting by an inverter that includes a first connection and a second connection, wherein the first connection is coupled to the source of the input stage, and wherein the second connection presents the input signal to the low-voltage flash memory device.

35. The method of claim 34, wherein inverting includes the inverter that includes an n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the input stage, wherein the source is coupled to ground, and wherein the drain presents an inverted input signal.

36. The method of claim 35, wherein inverting includes the inverter that further includes a p-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the input stage, wherein the drain is coupled to the drain of the n-channel transistor.

37. The method of claim 36, further comprising enabling the inverter by an enabling transistor having a gate, a drain, and a source, wherein the gate is receptive to an enabling signal, wherein the source is coupled to a voltage supply, wherein the drain is coupled to the drain of the p-channel transistor.

38. The method of claim 37, wherein enabling includes the enabling transistor that includes a p-channel transistor.

39. A method for buffering a low-voltage flash memory device, comprising:

transferring by an input stage having a first n-channel transistor that includes a gate, a drain, and a source, wherein the gate is receptive to an inhibiting signal, wherein the drain is receptive to an input signal, wherein transferring includes

inhibiting the input signal from being presented at the source when the inhibiting signal is at a low level;

outputting by an output stage to present the input signal to the low-voltage flash memory device, wherein outputting includes:

receiving the input signal by a second n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the first n-channel transistor, wherein the source is coupled to ground, and wherein the drain presents the input signal at a low level when the gate receives the input signal at a high level;

receiving the input signal by a first p-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the first n-channel transistor, and wherein the drain presents the input signal at a high level when the gate receives the input signal at a low level; and

enabling the first p-channel transistor by a second p-channel transistor having a gate, a drain, and a source, wherein the gate is receptive to a low enabling signal, wherein the source is coupled to a voltage supply, wherein the drain is coupled to the source of the first p-channel transistor.

40. The method of claim 39, wherein the act of inhibiting occurs when the low-voltage flash memory device is inactivated.

41. A method for buffering a low-voltage flash memory device, comprising:

transferring by an input stage having a first n-channel transistor that includes a gate, a drain, and a source, wherein the gate is receptive to an inhibiting signal, wherein the drain is receptive to an input signal, wherein the input stage refrains from transferring the input signal from being presented at the source when the inhibiting signal is at a low level;

outputting by an output stage to present the input signal to the low-voltage

flash memory device, wherein the output stage includes:

a second n-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the first n-channel transistor, wherein the source is coupled to ground, and wherein the drain presents an inverted input signal;

a first p-channel transistor having a gate, a drain, and a source, wherein the gate is coupled to the source of the first n-channel transistor, and wherein the drain is coupled to the drain of the second n-channel transistor; and

a second p-channel transistor having a gate, a drain, and a source, wherein the gate is receptive to an enabling signal, wherein the source is coupled to a voltage supply, wherein the drain is coupled to the source of the first p-channel transistor;

sensing by a voltage sensor to trigger when the input signal is at a first high level, wherein the voltage sensor is receptive to a pumped signal and the input signal to produce a sensed signal; and

producing by an inhibiting circuit that selectively produces the inhibiting signal, wherein the inhibiting circuit is receptive to the pumped signal and the sensed signal.

42. A wireless device, comprising:

a processor;

a display; and

a low-voltage flash memory device that includes:

a multiple of thin gate-oxide transistors; and

an input buffer receptive to an enabling signal, an input signal, and an inhibiting signal, wherein the input buffer includes a component that inhibits semiconductor breakdown of the multiple of thin gate-oxide transistors when

the inhibiting signal is at a predetermined level.

43. An input buffer protection circuit comprising:

an input node to receive an input signal;

an internal signal node coupled to communicate the input signal to an input buffer circuit;

a pass transistor coupled between the input node and the internal signal node;

a bias circuit coupled to the internal signal node, wherein the bias circuit and the pass transistor are coupled to be controlled by an inhibitor signal such that the bias circuit is active to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

control circuitry to provide the inhibitor signal.

44. The input buffer protection circuit of claim 43 wherein the control circuitry comprises transistors to deactivate the pass transistor and to activate the bias circuit when the input signal reaches a predetermined threshold voltage level.

45. The input buffer protection circuit of claim 43 wherein:

the pass transistor comprises an n-channel transistor comprising a gate coupled to receive the inhibitor signal, a drain, and a source; and

the bias circuit comprises a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node, gates of each of the pair of p-channel transistors being coupled to receive the inhibitor signal.

46. The input buffer protection circuit of claim 43 wherein the control circuitry comprises:

a voltage sensor coupled to receive a pumped signal and the input signal, the

voltage sensor to generate a sensed signal in response to the pumped signal and the input signal; and

an inhibiting circuit coupled to receive the pumped signal and coupled to the voltage sensor to receive the sensed signal, the inhibiting circuit being coupled to the pass transistor to generate the inhibitor signal in response to the pumped signal and the sensed signal.

47. An integrated circuit comprising:

an input node to receive an input signal;

an internal signal node coupled to communicate the input signal to an input buffer circuit;

a pass transistor coupled between the input node and the internal signal node;

a bias circuit coupled to the internal signal node, wherein the bias circuit and the pass transistor are coupled to be controlled by an inhibitor signal such that the bias circuit is active to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

control circuitry to provide the inhibitor signal to activate the pass transistor and deactivate the bias circuit while the input signal is less than a predetermined threshold voltage level, and to deactivate the pass transistor and activate the bias circuit when the input signal reaches the predetermined threshold voltage level.

48. The integrated circuit of claim 47 wherein:

the pass transistor comprises an n-channel transistor comprising a gate coupled to receive the inhibitor signal, a drain, and a source; and

the bias circuit comprises a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node, gates of each of the pair of p-channel transistors being coupled to receive the inhibitor signal.

49. The integrated circuit of claim 47 wherein the control circuitry comprises:

a voltage sensor coupled to receive a pumped signal and the input signal, the voltage sensor to generate a sensed signal in response to the pumped signal and the input signal; and

an inhibiting circuit coupled to receive the pumped signal and coupled to the voltage sensor to receive the sensed signal, the inhibiting circuit being coupled to the pass transistor to generate the inhibitor signal in response to the pumped signal and the sensed signal.

50. A memory device comprising:

an input node to receive an input signal;

an internal signal node coupled to communicate the input signal to an input buffer circuit;

a pass transistor coupled between the input node and the internal signal node;

a bias circuit coupled to the internal signal node, wherein the bias circuit and the pass transistor are coupled to be controlled by an inhibitor signal such that the bias circuit is active to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

control circuitry to provide the inhibitor signal to activate the pass transistor and deactivate the bias circuit while the memory device is in a non-test operation, and to deactivate the pass transistor and activate the bias circuit when the memory device is in a test mode indicated by an elevated voltage greater than a predetermined threshold voltage level provided on the input node.

51. The memory device of claim 50 wherein:

the pass transistor comprises an n-channel transistor comprising a gate coupled to receive the inhibitor signal, a drain, and a source; and

the bias circuit comprises a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node, gates of each of the pair of p-channel transistors being coupled to receive the inhibitor signal.

52. The memory device of claim 50 wherein the control circuitry comprises:

a voltage sensor coupled to receive a pumped signal and the input signal, the voltage sensor to generate a sensed signal in response to the pumped signal and the input signal; and

an inhibiting circuit coupled to receive the pumped signal and coupled to the voltage sensor to receive the sensed signal, the inhibiting circuit being coupled to the pass transistor to generate the inhibitor signal in response to the pumped signal and the sensed signal.

53. A method of operating an input buffer comprising:

receiving an input signal at an input node;

communicating the input signal to an input buffer circuit through an internal signal node;

controlling a pass transistor coupled between the input node and the internal signal node and a bias circuit coupled to the internal signal node with an inhibitor signal to activate the bias circuit to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

providing the inhibitor signal from control circuitry.

54. The method of claim 53 wherein controlling a pass transistor and a bias circuit further comprises deactivating the pass transistor and activating the bias circuit when the input signal reaches a predetermined threshold voltage level.

55. The method of claim 53 wherein:

controlling a pass transistor further comprises controlling an n-channel transistor comprising a gate, a drain, and a source by coupling the inhibitor signal to the gate of the n-channel transistor; and

controlling a bias circuit further comprises controlling a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node by coupling the inhibitor signal to gates of each of the pair of p-channel transistors.

56. The method of claim 53 wherein providing the inhibitor signal further comprises:

receiving a pumped signal and the input signal in a voltage sensor, and generating a sensed signal in the voltage sensor in response to the pumped signal and the input signal; and

receiving the pumped signal and the sensed signal in an inhibiting circuit, and generating the inhibitor signal in the inhibiting circuit in response to the pumped signal and the sensed signal.

57. A method of operating an integrated circuit comprising:

receiving an input signal at an input node;

communicating the input signal to an input buffer circuit through an internal signal node;

controlling a pass transistor coupled between the input node and the internal signal node and a bias circuit coupled to the internal signal node with an inhibitor signal to activate the bias circuit to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

providing the inhibitor signal from control circuitry to activate the pass

transistor and deactivate the bias circuit while the input signal is less than a predetermined threshold voltage level, and to deactivate the pass transistor and activate the bias circuit when the input signal reaches the predetermined threshold voltage level.

58. The method of claim 57 wherein:

controlling a pass transistor further comprises controlling an n-channel transistor comprising a gate, a drain, and a source by coupling the inhibitor signal to the gate of the n-channel transistor; and

controlling a bias circuit further comprises controlling a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node by coupling the inhibitor signal to gates of each of the pair of p-channel transistors.

59. The method of claim 57 wherein providing the inhibitor signal further comprises:

receiving a pumped signal and the input signal in a voltage sensor, and generating a sensed signal in the voltage sensor in response to the pumped signal and the input signal; and

receiving the pumped signal and the sensed signal in an inhibiting circuit, and generating the inhibitor signal in the inhibiting circuit in response to the pumped signal and the sensed signal.

60. A method of operating a memory device comprising:

receiving an input signal at an input node;

communicating the input signal to an input buffer circuit through an internal signal node;

controlling a pass transistor coupled between the input node and the internal

signal node and a bias circuit coupled to the internal signal node with an inhibitor signal to activate the bias circuit to bias the internal signal node to a predetermined voltage while the pass transistor is deactivated to interrupt a signal path from the input node to the internal signal node; and

providing the inhibitor signal from control circuitry to activate the pass transistor and deactivate the bias circuit while the memory device is in a non-test operation, and to deactivate the pass transistor and activate the bias circuit when the memory device is in a test mode indicated by an elevated voltage greater than a predetermined threshold voltage level provided on the input node.

61. The method of claim 60 wherein:

controlling a pass transistor further comprises controlling an n-channel transistor comprising a gate, a drain, and a source by coupling the inhibitor signal to the gate of the n-channel transistor; and

controlling a bias circuit further comprises controlling a pair of p-channel transistors and a resistor coupled in series between a voltage supply and the internal signal node by coupling the inhibitor signal to gates of each of the pair of p-channel transistors.

62. The method of claim 60 wherein providing the inhibitor signal further comprises:

receiving a pumped signal and the input signal in a voltage sensor, and generating a sensed signal in the voltage sensor in response to the pumped signal and the input signal; and

receiving the pumped signal and the sensed signal in an inhibiting circuit, and generating the inhibitor signal in the inhibiting circuit in response to the pumped signal and the sensed signal.

63. An input system for a low-voltage flash memory device, comprising:

an input buffer comprising:

an input stage comprising a transistor comprising a gate, a drain, and a source, the gate being coupled to receive an inhibiting signal and the drain being coupled to receive an input signal, the transistor being controlled to inhibit the input signal from being presented at the source when the inhibiting signal is at a first predetermined level; and

an output stage coupled to the input stage to present the input signal to the low-voltage flash memory device; and

a voltage sensor coupled to receive the input signal and a pumped signal to trigger when the input signal is at a second predetermined level.

64. The input system of claim 63 wherein:

the transistor comprises an n-channel transistor; and

the output stage comprises an inverter comprising a first connection and a second connection, the first connection being coupled to the source of the transistor and the second connection to present the input signal to the low-voltage flash memory device.

65. The input system of claim 63 wherein the voltage sensor comprises a triggering stage comprising a set of p-channel transistors and a set of n-channel transistors coupled to receive to the input signal.

66. The input system of claim 65 wherein the voltage sensor further comprises:

a set of metal options;

an inverting stage; and

a delay stage to reject undesired noise.

67. The input system of claim 63, further comprising an inhibiting circuit coupled to receive the pumped signal and coupled to the voltage sensor to receive a sensed signal generated by the voltage sensor, the inhibiting circuit being coupled to the input buffer to generate the inhibiting signal in response to the pumped signal and the sensed signal.

68. An input system for a low-voltage flash memory device, comprising:

an input buffer comprising:

an input stage comprising a transistor comprising a gate, a drain, and a source, the gate being coupled to receive an inhibiting signal and the drain being coupled to receive an input signal, the transistor being controlled to inhibit the input signal from being presented at the source when the inhibiting signal is at a first predetermined level; and

an output stage coupled to the input stage to present the input signal to the low-voltage flash memory device; and

an inhibiting circuit coupled to the input buffer to selectively produce the inhibiting signal, the inhibiting circuit being coupled to receive a pumped signal and a sensed signal.

69. The input system of claim 68 wherein:

the transistor comprises an n-channel transistor; and

the output stage comprises an inverter comprising a first connection and a second connection, the first connection being coupled to the source of the transistor and the second connection to present the input signal to the low-voltage flash memory device.

70. The input system of claim 68, wherein the inhibiting circuit comprises:

a first n-channel transistor comprising a gate coupled to receive the sensed

signal, a drain coupled to present the inhibiting signal, and a source coupled to ground;

a second n-channel transistor comprising a gate coupled to an inverted sensed signal, a drain, and a source coupled to ground;

a first p-channel transistor comprising a gate coupled to the drain of the second n-channel transistor, a drain coupled to the drain of the first n-channel transistor, a source coupled to receive the pumped signal, and a bias coupled to receive the pumped signal; and

a second p-channel transistor comprising a gate coupled to the drain of the first n-channel transistor, a drain coupled to the drain of the second n-channel transistor, a source coupled to receive to the pumped signal, and a bias coupled to receive the pumped signal.

71. The input system of claim 26, further comprising a voltage sensor coupled to receive the pumped signal and the input signal, the voltage sensor to generate the sensed signal, the inhibiting circuit being coupled to the voltage sensor to generate the inhibiting signal in response to the pumped signal and the sensed signal.